AMENDMENTS

In the Specification

Please substitute the following amended paragraph for the Abstract of the Disclosure:

A digital adjustable chip oscillator ~~comprising: a voltage control oscillator generating an oscillation signal, receiving a control voltage to adjust the frequency of the oscillation signal, and receiving an operating voltage to stabilize the frequency of the oscillation signal; a reference voltage circuit generating a reference voltage; a voltage regulation circuit receiving the reference voltage and generating the operating voltage; a digital tuning circuit receiving a digital code to adjust the control voltage and receiving the operating voltage to stabilize the control voltage; a frequency detector receiving the oscillation signal, a first reference signal with a first frequency, and a second reference signal with a second frequency, wherein when the frequency of the oscillation signal lies between the first frequency and the second frequency, the frequency detector will output a high voltage comparison signal, otherwise the frequency detector will output a low voltage comparison signal; a programmable counter receiving a clock signal to trigger the counting and generating the digital code; a programmable controller receiving the high voltage comparison signal to generate an enable signal directing the frequency detector to hold the high voltage comparison signal and directing the programmable counter to stop counting and hold the digital code; and a programmable memory receiving the enable signal to record the digital code~~ comprises a voltage control oscillator, a reference voltage circuit, a voltage regulation circuit, a digital tuning circuit, a frequency detector and a programmable controller. The oscillator generates an oscillation signal and receives a control voltage and an operating voltage from the voltage regulation circuit and the reference voltage circuit to stabilize and adjust

the frequency of oscillation signal. The digital tuning circuit receives a digital code stored in a programmable memory to adjust the control voltage. The frequency detector detects and compares the frequency of oscillation signal with a first and second frequency, wherein when the frequency of the oscillation signal lies between the first and second frequency, the frequency detector outputs a high voltage signal and otherwise the frequency detector outputs a low voltage signal. The programmable controller receives the high voltage signal to stop a programmable counter to acquire the digital code.